STREAMLINED FIELD ISOLATION PROCESS

Field of the Invention

The invention relates generally to silicon integrated circuit fabrication. In particular, the invention pertains to the device isolation processes involving the local oxidation of silicon.

Background of the Invention

Implementing electric circuits in an integrated process involves connecting isolated devices through specific electrical paths. In silicon ultra large scale integration, effective device isolation becomes increasingly important as device dimensions become smaller and packing density rises.

In conventional Metal-Oxide-Silicon (MOS) device fabrication, device isolation is often implemented by means of recessed or semi-recessed silicon dioxide (SiO_2 or "oxide") regions in the non-active or field areas of the silicon substrate. This so-called Local Oxidation of Silicon (LOCOS) has become the most widely used isolation technology. In various forms, it remains the technique of choice for MOS device isolation.

A basic LOCOS process begins with the formation of a relatively thin (20-60 nm) pad-oxide layer over substantially an entire clean silicon (Si) wafer. Following the pad-oxide deposition, a silicon nitride (Si_3N_4 or "nitride") layer of about 100-200 nm thick is deposited. Subsequently, the wafer is masked and the nitride/pad-oxide is etched to define the active regions. The exposed regions are the inactive or field regions wherein the field oxide is grown. Prior to oxide growth, optional dopant implants may be carried out to create channel-stops located beneath the field oxide. The field oxide is typically thermally grown at about atmospheric pressure by means of wet oxidation, at temperatures of about 1000°C for 2-4 hours, resulting in oxide thicknesses in the range of 0.3-1.0 μm. Dry oxidation is usually not preferred because of the generally low oxidation rate which adds considerably to process throughput.

Even though the oxide grows substantially only within the regions defined by the masking nitride, some oxidant may diffuse laterally causing excess oxide to grow under the edges of the nitride mask, often forming a so-called "bird's beak" effect.

The bird's beak presents several problems for device isolation. Modifications of the basic LOCOS isolation process have succeeded in reducing the bird's beak considerably.

During the growth of the field oxide, another phenomenon occurs that causes defects in the structure, which later become detrimental to the thin gate oxide. Kooi, et al. (J. Electrochem. Soc., vol. 123, pp. 1117, 1976), discovered that a thin layer of silicon nitride can form on the silicon surface at the pad-oxide/silicon interface as a result of the reaction of ammonia (NH_3) and silicon. The ammonia is generated from the reaction between water vapor (H_2O) and the masking nitride during the field-oxidation step. The ammonia diffuses through the pad oxide and reacts with the silicon substrate to form silicon nitride spots or ribbons, sometimes called the *white ribbon* effect. Subsequently, when the gate oxide is grown, the growth rate becomes impeded at the locations where the silicon nitride has formed. The gate oxide is thus thinner at these locations than elsewhere, causing low-voltage breakdown of the gate oxide. One common way to eliminate this problem is to grow a "sacrificial" oxide layer after etching the masking nitride and pad-oxide layers. The sacrificial oxide is then removed before growing the final gate oxide. Clearly, however, the additional processes involved for eliminating the Kooi effect adds to the cost and complexity of ULSI fabrication.

Summary of the Invention

It is an object of the present invention to provide a field isolation process which obviates the need for sacrificial oxide growth and removal to eliminate parasitic silicon nitride inclusions. It is a further object of the present invention to provide a field oxidation process which prevents the formation of silicon nitride inclusions at the silicon/silicon dioxide interface. It is yet another object of the present invention to provide a field oxidation process which eliminates the use of hydrogen-containing oxidants, thereby preventing silicon nitride formation concurrent with the field oxide formation and achieve the requisite field oxide growth.

In accordance with one aspect of the present invention, a field isolation process comprises growing a field oxide region on a semiconductor wafer by means of a hydrogen-free oxidant. Preferably the oxidant comprises substantially only oxygen

and the field oxide process is preferably carried out at oxygen partial pressures greater than 10 atm and temperatures greater than about 900 °C.

In accordance with another aspect of the present invention, a method of growing a field oxide region on a semiconductor wafer comprises growing a first portion of the field oxide region by means of exposing a portion of the wafer to a first oxidizing ambient comprising water vapor. The field oxide region is completed by further exposing the portion of the wafer to a second oxidizing ambient comprising oxygen.

In accordance with yet another aspect of the present invention, a field isolation region on a semiconductor substrate is formed by a process comprised of exposing the field region of the semiconductor wafer to an oxidizing ambient comprising substantially only oxygen. More preferably, the isolation region is first exposed to an oxidizing ambient comprising at least in part water vapor, and subsequently exposed to the oxidizing ambient comprised of substantially only oxygen.

These as well as other objects and attributes of the present invention will become more fully apparent from the following description with reference to the accompanying drawings.

Brief Description of the Drawings

Figures 1A-1H is a schematic partial process flow illustrating a representative field isolation process and the accompanying Kooi effect.

Figure 2A-2B is a schematic partial process flow illustrating a field oxide grown by high pressure oxidation.
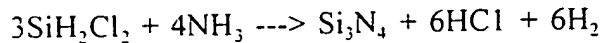
Figure 3A-3C is a schematic partial process flow illustrating a field oxide with encapsulated parasitic nitride.

Detailed Description of the Invention

As shown in Figure 1A, an exemplary conventional LOCOS process begins by depositing a buffer or pad-oxide layer (SiO_2) 14 of about 20-60 nm thick on a clean surface of a silicon wafer 12. The pad-oxide provides a stress relief buffer between the silicon surface and an overlaying silicon nitride layer. As shown in Figure 1B, a layer of silicon nitride 16 of about 100-200 nm thick is deposited on the pad-oxide. Silicon nitride is typically deposited by a chemical vapor deposition (CVD) of
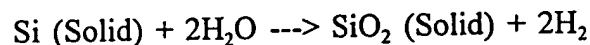
dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) at temperatures between 700°C and 800°C, according to the overall reaction:

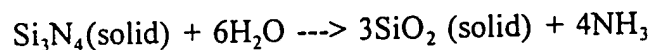$$3SiH_2Cl_2 + 4NH_3 \longrightarrow Si_3N_4 + 6HCl + 6H_2$$

A photolithographic process is then used to define the active regions. A resist pattern is normally used to protect all of the areas where the active devices will be formed. The nitride layer is then dry etched and the pad-oxide is etched by either a wet-or-dry-chemical process. Figure 1C illustrates an exemplary structure resulting from the masking and etch process. After the mask and etch process, optional dopant implants may be formed in the field regions, creating a channel-stop 20, as shown in Figure 1D. The channel-stop 20 is intended to provide enhanced device isolation and is thus mentioned by way of example as a common practice in LOCOS process integration. Moreover, the channel-stop implant 20 may be performed in other ways, for example after field oxide growth. It will be appreciated that such channel-stop implant processes may be integrated in a variety of ways, and are optional in the context of the present invention.

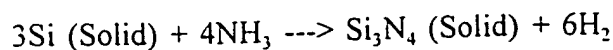The field oxide is thermally grown by means of wet oxidation according to the general formula:

$$Si \text{ (Solid)} + 2H_2O \longrightarrow SiO_2 \text{ (Solid)} + 2H_2$$

Typical field oxide layers 22 as shown in Figure 1E are grown to thicknesses of about 0.3 to 1.0 µm. Wet oxidation is typically carried out at temperatures in the range of 900°C to 1200°C and oxidant partial pressures from about 0.2 to 25 atm. As a silicon oxidant, water vapor is conventionally preferable because of the generally high oxidation rate.

However, during growth of the field oxide 22, a parasitic inclusion of silicon nitride can form at the silicon/pad-oxide interface as a result of the reaction of released ammonia with silicon. Specifically, ammonia is released by the reaction of Si_3N_4 (Solid) and H_2O present during wet oxidation according to the approximate formula:

$$Si_3N_4 \text{(solid)} + 6H_2O \longrightarrow 3SiO_2 \text{ (solid)} + 4NH_3$$

Ammonia released by the reaction diffuses through the SiO_2 pad-oxide layer and reacts with the silicon substantially at the Si/SiO_2 interface according to the general formula:

$$3Si \text{ (Solid)} + 4NH_3 \longrightarrow Si_3N_4 \text{ (Solid)} + 6H_2$$

As shown in Figure 1E. the parasitic nitride inclusions 24 generally grow at the Si/SiO₂ interface adjacent to the field oxide 22. Subsequent nitride and pad-oxide etching processes leave the surface of the silicon substrate exposed for further processing. However, the nitride inclusions 24 are also present at the silicon surface, as illustrated in Figure 1F. Further processing is compromised by the presence of the nitride inclusions 24. For example, subsequent growth of a gate oxide layer requires a thin, high quality oxide having uniform thickness and composition. The nitride inclusions 24 cause the gate oxide to become thinner in these regions which ultimately contributes to device breakdowns. Thus, additional processing is needed to alleviate this problem.

As shown in Figure 1G, typically a sacrificial oxide layer 26 is grown over the silicon surface to an extent which substantially oxidizes the nitride inclusions 24. The sacrificial oxide 26 is then etched, leaving a silicon surface and field oxide 22 substantially free of the nitride inclusions 24, as illustrated in Figure 1H. The aforementioned sacrificial oxide growth and removal have, conventionally, been considered necessary process steps for alleviating the Kooi effect.

In accordance with the principles of the present invention, a preferred isolation process comprises utilizing a high pressure field oxidation (HiPox) process using an oxidant substantially free of hydrogen. In this respect, it is preferable to perform a field HiPox process using an oxidant such as oxygen (O_2) in place of H_2O. Performing the oxidation of silicon at high pressure significantly enhances the oxidation rate, thus compensating a possible lower oxidation rate of O_2 relative to that of H_2O. Performing a field oxidation using an oxidant, substantially free of hydrogen, such as substantially pure oxygen prevents formation of silicon nitride inclusions via the Kooi effect.
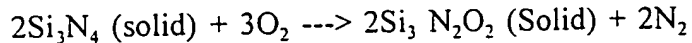
One embodiment of a preferred field oxidation process is illustrated in Figures 2A-2B. Figure 2A illustrates a wafer section processed up to the point of field oxidation. Previous processing steps may be substantially equivalent to that described in connection with Figures 1A-1D. As shown in Figure 2A, a starting structure may comprise the silicon substrate 12, pad-oxide layer 14, nitride mask 18 and optional channel-stop implant 20. Figure 2B illustrates the result of a high pressure field

oxidation using O_2 as the oxidant. The field oxide 20 is grown substantially similar to that described previously in connection with Figure 1E, except that the nitride inclusions 24 are eliminated.

A preferred HiPox process using O_2 follows the general formula:

$$Si \text{ (solid)} + O_2 \text{ ---> } SiO_2 \text{ (solid)}$$

It is possible that nitrogen (N_2) may be released in a possible accompanying reaction of O_2 with the masking nitride 18 according to the following approximate reaction or variations from stoichiometry thereof:

$$2Si_3N_4 \text{ (solid)} + 3O_2 \text{ ---> } 2Si_3 N_2O_2 \text{ (Solid)} + 2N_2$$

However, N_2 does not react significantly with the underlying silicon, as does the NH_3 released in the prior art field oxidation. A HiPox field oxidation is generally performed at partial pressures in the range of 5 atm to 30 atm, and in a temperature range of 900 °C to 1200 °C. Resulting oxidation rates may range from 2 nm/min. to 8 nm/min. Preferable HiPox processes are performed at O_2 partial pressures of about 25 atm, at 1000 °C resulting in oxidation rates of about 5 nm/min.

Having a field oxide substantially free of nitride inclusions 26 (Figure 1), allows subsequent processing without the need for sacrificial oxide growth as discussed in connection with Figures 1G and 1H.

Another preferred field oxidation process comprises a two-step operation, whereby an initial field oxide is grown by wet oxidation followed by a HiPox oxidation step. As shown in Figure 3A, a possible starting structure may comprise the result of prior processing steps as described in connection with Figures 1A-1D. As shown in Figure 3B, a first partial field oxide 28 is grown by wet oxidation, as previously described in connection with Figure 1E. The wet oxidation process, however, produces residual nitride inclusions 30. A second field oxidation is then performed by HiPox using an O_2 oxidant. As shown in Figure 3C, the HiPox step substantially completes the field oxide 32, and grows an oxide which consumes the nitride inclusions 30. Since the nitride inclusions are no longer located at the Si/SiO_2 interface, their influence on subsequent processing steps is ameliorated. Advantages of the present embodiment include use of the relatively inexpensive and efficient wet

oxidation to create a portion of the field oxide, minimizing the more expensive HiPox process and eliminating the need for the sacrificial oxide.

Although described above with reference to the preferred embodiments, modifications within the scope of the invention may be apparent to those skilled in the art, all such modifications are intended to be within the scope of the appended claims.